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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,686	11/04/2003	Wolfgang Korber	Q78259	4926

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EXAMINER	
WONG, XAVIER S	

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2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,686	KORBER ET AL.	
	Examiner	Art Unit	
	Xavier Szewai Wong	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2nd August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10th August 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) ✓

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

- Applicant's Amendment filed 2nd *August 2007* is acknowledged
- Claims **7**, **12**, and **16** have been amended
- Claims **1-16** are still pending in the present application
- This action is made NON-FINAL

Drawings

The drawings were received on *10th August 2007*. These drawings are accepted.

Claim Rejections - 35 USC § 112

Applicant's arguments (see pg. 2), filed 2nd *August 2007*, with respect to 35 U.S.C § 112 rejections have been fully considered and are persuasive. The 112 rejections of claims **11** and **16** have been withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims **1**, **5**, **8**, **9**, **10**, **13** and **14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**).

Consider claim **1**, **Nong** discloses a multi-channel network node (fig. 2 @ *111*) for routing and switching data from a number of input ports (fig. 2 @ input ports) to a number of output ports (fig. 2 @ output ports). Data is buffered in an input port wherein the data is organized into physical buffers ([0057]: 14-18; fig. *5* @ buffers B11-B14); each of the buffer being assigned to a destined output port (fig. *4* @ buffers B11-B14); a switch fabric (fig. 2 @ *230*) that routes the data from the input port (comprising the data buffers) to the output port ([0057]: 8-12). **Nong** may not have explicitly disclosed a (single) "memory unit" organized as a number of physical queues; nonetheless, it would have been obvious to one of ordinary skill in the art when the invention was made to consider the input port

(out of a plurality of input ports) of **Nong** as the memory unit comprising a number of data buffers for assigning data in specific input queues to be routed to specific output queues.

Consider claim **5**, as applied to claim **1**, **Nong** shows in figure *8* (input port / memory unit) and figure *9* (output port / memory unit) input/output buffer managers (agents) *815* & *910*. The managers control the operations of the buffers ([0120,0125,0128; 0142,0146-148]).

Consider claim **8**, as applied to claim **1**, **Nong** shows in figure *3* a crossbar (matrix) switch *230* ([0052]).

Consider claim **9**, as applied to claim **1**, **Nong** discloses in figure *2* a scheduling controller *240* for controlling the switch *230* ([0051]: 4-14), which is a processor obviously controlled by software.

Consider claim **10**, as applied to claim **1**, **Nong** shows in figures *4*, *5* and *6* that input and output interfaces are assigned to the input and output ports respectively.

Consider claim **13**, as applied to claim **1**, **Nong** shows in figure *2* that node *111* output ports output data through speed-data paths (OSUDP) and subsequently in figure *1*, node *111* output data to an end user e.g. *132* or another node e.g. *112*. The output ports, thus, are output ports of the network node *111*.

Consider claim **14**, **Nong** discloses a multi-channel network node (fig. *2* @ *111*) for routing and switching data from any input port to any output port (figs. *4-6*) comprising steps of: queuing data into an input port wherein the data is organized into physical buffers ([0057]: 14-18; fig. *5* @ buffers B11-B14); each of the buffer being

assigned to a destined output port (fig. *4* @ buffers B11-B14); a switch fabric (fig. *2* @ *230*) that routes the data from the input port (comprising the data buffers) to the output port ([0057]: 8-12). **Nong** may not have explicitly disclosed receiving data from a data channel by a *receiver unit*; or, the buffers (queues) constituting a "memory unit"; nonetheless, it would have been obvious to one of ordinary skill in the art when the invention was made to consider the input port of **Nong** as the receiver and memory unit comprising a number of data buffers for similar reasons of receiving and assigning data in specific input queues to be routed to specific output queues.

Claims **2** and **15** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Bohm** et al (**US 2002/0027816 A1**).

Consider claims **2** and **15**, as applied to claims **1** and **14**, **Nong** discloses the claimed invention except explicitly mentioning the memory queues comprising a number of coherent memory cells. **Bohm** et al disclose utilizing coherent memory cells array ([0055]: 7-12). It would have been obvious to one of ordinary skill in the art when the invention was made to incorporate the coherent memory cells of **Bohm** et al to the memory buffers of **Nong** for providing sufficient space for carrying out read/write operations in switches.

Claim **3** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Bohm** et al (**US 2002/0027816 A1**), as applied to claim **2**, and in further view of **Strehler** (**US 5,122,984**).

Consider claim **3**, as applied to claim **2**, **Nong**, as modified by **Bohm** et al, disclose the claimed invention except explicitly mentioning resizable memory cells. **Strehler** teaches the concept of sizable (re-sizable) memory cells (col. 1: 28-38). It would have been obvious to one of ordinary skill in the art when the invention was made to incorporate the teachings of **Strehler** to the invention of **Nong**, as modified by **Bohm** et al, for organizing data structures to be stored (e.g. redistributing capacity among cells).

Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Kothary** (**US 6,249,528 B1**).

Consider claim **4**, as applied to claim **1**, **Nong** discloses the claimed invention except specifying a re-assembly unit coupled to the input ports of the node and the switch; and a segmentation unit with the memory unit and output ports of the node. **Kothary** shows in figure *2* a re-assembly unit coupled to a switch unit, which is coupled to a segmentation unit. The re-assembly unit in figure *13* and the segmentation unit in figure *14* both show FIFO buffers (memory units) *152* and *166* respectively (col. 13: 52-67; col. 14: 42-57). It would have been obvious to one of ordinary skill in the art when the invention was made to incorporate the memory unit / re-assembly / segmentation units of **Kothary** to the invention of **Nong** for cell re-assembly and segmentation purposes.

Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Dooley** et al (**US 2002/0163922 A1**).

Consider claim **6**, as applied to claim **5**, **Nong** discloses the claimed invention except may not have *explicitly* shown the memory queue and agents form the switching unit. **Dooley** et al disclose an input switch port (fig. *1* @ *14*) comprise a traffic manager (fig. *2A* @ *22* → *agent*) and inside of the traffic manager comprises memory queues (fig. 3 @ 37) which leads to the switch interface (fig. *2* @ *24*) and eventually to the switch (fig. *1* @ *16*) ([0026]). It would have been obvious to one of ordinary skill in the art when the invention was made to incorporate the input switch port of **Dooley** et al to the node of **Nong** so the queues coordinate with the traffic manager to switch the queues to the corresponding output ports.

Claim **7** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong** (**US 2003/0123468 A1**) in view of **Fujii** et al (**US 2003/0014264 A1**).

Consider claim **7**, as applied to claim **5**, **Nong** discloses the claimed invention except specifically mentioning the memory queues and agent operate *asynchronously* and *in parallel*. **Fujii** et al disclose an input/output processing unit (control / agent) asynchronously inputs data stream into a FIFO memory queue in a decode processing unit wherein both input/output and decode processing units operate in parallel to each other ([0212]). It would have been obvious to one of ordinary skill in the art to apply the concept of a control unit operating asynchronously and in parallel with a queue as taught by **Fujii** et al to the buffers and manager (agent) of **Nong** for efficient parallel processing of data.

Claims **11** and **12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong (US 2003/0123468 A1)** in view of **Liebowitz** et al **(US 5,757,784)**.

Consider claim **11**, as applied to claim **1**, **Nong** discloses the claimed invention except explicitly mentioning a burst buffer being utilized in the node. **Liebowitz** et al disclose in figure *4* the usage of burst buffer *68* in a fragment assembler/disassembler FAD *66* (col. 4: 19-41). It would have been obvious to one of ordinary skill in the art when the invention was made to combine the burst buffer of **Liebowitz** et al to the node of **Nong** for efficiently handling different data sizes and formats.

Consider claim **12**, as applied to claim **11**, **Nong**, as modified by **Liebowitz** et al, shows in figures *2* that the output port *220* (fig. *9* output port → memory unit) is coupled with switch *230*.

Claim **16** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nong (US 2003/0123468 A1)** in view of **Moriwaki** et al **(EP 0,918,419 A2)**.

Consider claim **16**, and as applied to claim **1**, **Nong** discloses the claimed invention except specifically disclosing a network of interactive *cascaded* multi-channel nodes. **Moriwaki et al** teach the concept of different levels of inputs and outputs in the ATM switch system from the input highways of the cell distributors to the ATM switches to the output highways of the cell assemblers; therefore, creating a cascade of devices operating in a succession of stages (col. *3* lines *52-58* & col. *4* lines *1-46*; fig. *1*). The ATM switch units exchange (interaction) cells with other ATM switch units in an N x N switch matrix (col. *6* lines *6-39*; *abstract*; fig. *1*). It would have been obvious to one of

ordinary skill in the art when the invention was made to apply the concept of **Moriwaki** et al to the invention of **Nong** for inter-node communications.

Response to Arguments

Applicant's arguments with respect to claims **1**, **3**, **4**, **6**, **11** and **14** have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wills (US 6,052,376) mentions ATM switch for transferring cells from input channels to output channels. Backpressure signal is utilized to handle congestion.

This action is made NON-FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xavier Wong whose telephone number is 571-270-1780. The examiner can normally be reached on Monday through Friday 8 am - 5 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Xavier Szewai Wong
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28th October 2007

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